REMARKS

Favorable reconsideration of this application, as amended, is respectfully requested.

The rejections under 35 U.S.C. §§ 102(b) and 103(a) are respectfully traversed.

As recited in independent Claim 1, first and second connecting areas are formed between respective first and second memory areas and a sense amplifier area. This important feature of Applicants' invention (discussed in the specification without limiting the claims) is neither taught nor suggested by Nakano relied on in the rejections.

As stated on page 4 of Applicants' specification:

> In the inventive semiconductor integrated circuit device, first data lines which are formed on a first layer and first lines which are formed on a second layer different from the first layer are connected in a first connecting area between a first memory array area and a sense amplifier area, and second data lines which are formed on the first layer and second lines which are formed on the second layer are connected in a second connecting area between a second memory array area and the sense amplifier area. This layout scheme can reduce the line interval of the first and second lines which are connected to the first and second data lines, respectively.

As further stated on page 30 of Applicants' specification:

> According to the present invention, the bit lines (data lines) BL (e.g., BL2a) which are formed on the first layer and the second-layer lines M2 (e.g., M2a) which are formed on the second layer different from the first layer are connected in the first connecting area

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between the first memory cell forming area and the sense amplifier area, and the bit lines BL (e.g., BL1c) which are formed on the first layer and the second-layer lines M2 (e.g., M2c) which are formed on the second layer are connected in the second connecting area between the second memory cell forming area and the sense amplifier area, whereby it is possible to reduce the interval of the second-layer lines which are connected to the respective bit lines.

To assist in an understanding of important differences between Applicants' invention and the prior art, three sketches are submitted herewith. Sketch 1 is based on Fig. 1 of Applicants' drawings marked up to emphasize features of the invention. Sketch 2 is based on Fig. 5 of Applicants' drawings, similarly marked up to emphasize features of Applicants' invention. These sketches are not intended to limit the scope of Applicants' claims.

Sketch 3 is based on sheet 12 of the drawings of the Nakano reference. By comparing sketches 1 and 2 with sketch 3, significant differences between Applicants' invention and Nakano are immediately apparent. In particular, in the Nakano reference, there is a connecting area in a sense amplifier area, unlike Applicants' invention. Thus, the advantages of Applicants' invention specified earlier are not achieved by Nakano.

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Accordingly, independent Claim 1 and dependent Claims 2-12 should be allowed. This application is now believed to be clearly in condition for allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on February 2, 2004.

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